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EXAMINER	
PETRANEK, JACOB ANDREW	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,216	CHAUVEL ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 are pending.

2. The office acknowledges the following papers:

Specification, claims, arguments, and drawings filed on 7/17/2006.

Withdrawn objections and rejections

3. The specification objections have been withdrawn due to amendment.

4. The drawing objections have been withdrawn due to amendment.

5. The claim objection for claim 3 has been withdrawn due to amendment.

6. The claim rejection for claim 3 has been withdrawn due to amendment.

Maintained Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

8. Claims 10 and 13 are rejected under 35 U.S.C. §102(e) as being anticipated by Gee (U.S. 6,317,872).

9. As per claim 10:

Gee disclosed a method comprising:

Fetching an instruction (Gee: Figure 1 element 104, column 8 lines 63-67)(The instructions are fetched from element 104); and

Determining whether said instruction is to be executed or replaced by a group of other instructions (Gee: Figure 2 element 200, column 9 lines 5-52)(The control store contains the micro sequence for each macro java bytecode and is used to replace the bytecode.).

10. As per claim 13:

Gee disclosed the method of claim 10 further including switching an active program counter between two program counters when replacing the instruction with the group of instructions (Gee: Figure 2 element 204 and 226, column 8 lines 49-67 continued to column 9 lines 1-52)(The primary program counter, element 204, is functioning to fetch java bytecodes and the micro program counter, element 226, is selected to fetch and execute the micro program. Thus having the same functionality.).

11. Claims 10-12, 14, and 22-23 are rejected under 35 U.S.C. §102(e) as being anticipated by Zaidi (U.S. 6,581,154).

12. As per claim 10:

Zaidi disclosed a method comprising:

Fetching an instruction (Zaidi: Figure 1 element 100, column 3 lines 22-33); and

Determining whether said instruction is to be executed or replaced by a group of other instructions (Zaidi: Figure 2 element 203, column 3 lines 55-67 continued to

column 4 lines 1-7)(The micro instruction sequencer logic determines if the instruction is a Uop or a S Uop that will further be expanded and replaced by a group of instructions.).

13. As per claim 11:

Zaidi disclosed the method of claim 10 further including replacing the instruction with said group of other instructions (Zaidi: Figure 2 element 210, column 3 lines 55-67 continued to column 4 lines 1-7)(The micro instruction sequencer logic determines if the instruction is a Uop or a S Uop that will further be expanded and replaced by a group of instructions.).

14. As per claim 12:

Zaidi disclosed the method of claim 10 wherein determining whether the instruction is to be executed or replaced includes determining a value of a bit associated with the instruction (Zaidi: Figure 2 element 205, column 4 lines 1-7)(Element 205 stores both U ops and S U ops. The S U ops are to be further expanded and the bits associated with them indicate that they are to be replaced by a group of instruction by element 210. The U ops have bits associated with them that indicate no further expansion is needed and that they can be sent directly to the dispatch queue. Thus having the same functionality.).

15. As per claim 14:

Zaidi disclosed the method of claim 10 further including programming a table to specify which instructions are to be executed directly and which instructions are to be replaced by a group of instructions (Zaidi: Figure 2 element 205, column 4 lines 1-7)(Element 205 stores both U ops and S U ops. The S U ops are to be further

expanded and the bits associated with them indicate that they are to be replaced by a group of instruction by element 210. The U ops have bits associated with them that indicate no further expansion is needed and that they can be sent directly to the dispatch queue. Thus having the same functionality.).

16. As per claim 22:

Zaidi disclosed a processor, comprising:

Decode logic that decodes instructions (Zaidi: Figure 1 element 110, column 3 lines 34-39); and

A means for determining whether an instruction is to be executed or replaced by a micro-sequence of other instructions (Zaidi: Figure 2 element 203, column 3 lines 55-67 continued to column 4 lines 1-7)(The micro instruction sequencer logic determines if the instruction is a Uop or a S Uop that will further be expanded and replaced by a group of instructions.).

17. As per claim 23:

Zaidi disclosed the processor of claim 22 further including a means for replacing the instruction with the micro-sequence (Zaidi: Figure 2 element 203, column 3 lines 55-67 continued to column 4 lines 1-7)(The micro instruction sequencer logic determines if the instruction is a Uop or a S Uop that will further be expanded and replaced by a group of instructions.).

18. Claims 18 and 21 are rejected under 35 U.S.C. §102(e) as being anticipated by Seal et al. (U.S. 6,965,984).

19. As per claim 18:

Seal disclosed an electronic device, comprising:

Decode logic that decodes instructions (Seal: Figure 1 element 10, column 6 lines 20-28); and

A vector table comprising a plurality of entries, each entry corresponding to a separate instruction and including a first field indicating whether the corresponding instruction is to be executed by the electronic device or whether the instruction is to be replaced by a predetermined group of instructions stored in memory (Seal: Figure 2 element 24, column 6 lines 60-67 continued to column 7 lines 1-23)(All of the entries in element 24 store pointers to a group of instructions that will replace the instruction. Thus having the same functionality.).

20. As per claim 21:

Seal disclosed the electronic device of claim 18 wherein the group of instructions terminates with a predetermined instruction (Seal: Figure 2 element 26, column 7 lines 24-40)(The BXJ instruction will cause a group of instructions to terminate. Thus having the same functionality.).

Maintained Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claims 18-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Gee et al. (U.S. 6,317,872), in view of Seal et al. (U.S. 6,965,984).

23. As per claim 18:

Gee disclosed an electronic device, comprising:

Decode logic that decodes instructions (Gee: Figure 1 element 100, column 8 lines 63-67)(The instructions are executed and thus inherently must be decoded first.)

Gee failed to teach a vector table comprising a plurality of entries, each entry corresponding to a separate instruction and including a first field indicating whether the corresponding instruction is to be executed by the electronic device or whether the instruction is to be replaced by a predetermined group of instructions stored in memory.

However, Seal disclosed a vector table comprising a plurality of entries, each entry corresponding to a separate instruction and including a first field indicating whether the corresponding instruction is to be executed by the electronic device or whether the instruction is to be replaced by a predetermined group of instructions stored in memory (Seal: Figure 2 element 24, column 6 lines 60-67 continued to column 7 lines 1-23)(All of the entries in element 24 store pointers to a group of instructions that will replace the instruction. Thus having the same functionality.).

Gee disclosed a processor that replaces macro java bytecodes with a micro sequence of instructions. Gee disclosed that a java bytecode is essentially a pointer to a sequence of microinstructions (Gee: Column 8 lines 57-59). However, Gee doesn't disclose the process of the replacement. One of ordinary skill in the art would have been motivated by the lack of the disclosure on the replacement process to find

additional details on the process. Seal disclosed using a vector table of entries that will replace java bytecodes. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a vector table to contain pointers to the micro instructions that will replace the java bytecodes.

24. As per claim 19:

Gee and Seal disclosed the electronic device of claim 18 further including an active program counter selected as either a first program counter or a second program counter, wherein an instruction is replaced by the group of instructions and the active program counter concurrently switches from the first to the second program counter (Gee: Figure 2 element 204 and 226, column 8 lines 49-67 continued to column 9 lines 1-52)(The primary program counter, element 204, is functioning to fetch java bytecodes and the micro program counter, element 226, is selected to fetch and execute the micro program. Thus having the same functionality.).

25. As per claim 20:

Gee and Seal disclosed the electronic device of claim 18 wherein upon switching the active program counter, the first program counter is incremented (Gee: Figure 2 elements 204 and 236, column 8 lines 49-67 continued to column 9 lines 1-52)(When another macro instruction is to be fetched from memory, the PC is incremented to insure that the correct instruction is fetched instead of an instruction previously fetched. Thus having the same functionality.).

New Claim Rejections - 35 USC § 103

26. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

27. Claims 1-4 and 7-9 is rejected under 35 U.S.C. §103(a) as being unpatentable over Gee et al. (U.S. 6,317,872), in view of Seal (U.S. 6,965,984).

28. As per claim 1:

Gee disclosed a processor comprising:

Fetch logic that retrieves instructions from memory (Gee: Figure 1 element 104, column 8 lines 63-67)(The instructions are fetched from element 104);

Decode logic coupled to said fetch logic (Gee: Figure 1 element 100, column 8 lines 63-67)(The instructions are executed and thus inherently must be decoded first.);

An active program counter selected as either a first program counter or a second program counter (Gee: Figure 2 element 204 and 226, column 8 lines 49-67 continued to column 9 lines 1-52)(The primary program counter, element 204, is functioning to fetch java bytecodes and the micro program counter, element 226, is selected to fetch and execute the micro program. Thus having the same functionality.); and

Wherein an instruction is replaced by a micro-sequence comprising one or more instructions and the active program counter switches between the first and second program counters (Gee: Figure 2 element 204 and 226, column 8 lines 49-67 continued to column 9 lines 1-52)(The primary program counter, element 204, is functioning to

fetch java bytecodes and the micro program counter, element 226, is used to fetch and execute the micro program. Thus having the same functionality.).

Gee failed to teach wherein an instruction is replaced by a micro-sequence comprising one or more instructions and the active program counter switches between the first and second program counters based on a micro-sequence-active bit.

However, Seal disclosed wherein an instruction is replaced by a micro-sequence comprising one or more instructions and the active program counter switches between the first and second program counters based on a micro-sequence-active bit (Seal: Figure 2 elements 22-26, column 6 lines 10-28 and lines 60-67 continued to column 7 lines 1-40)(The combination of Seal and Gee allows for instructions to not be replaced by a sequence of microoperations for the processor of Gee. This results in the processor of Gee not always needing to run the microPC because there won't always be instructions that need to be replaced by a sequence of microoperations. Thus, it would have been obvious to one of ordinary skill in the art that with the combination, there should be a status bit to tell the microPC to stop incrementing when there aren't any instructions to fetch that are being replaced by a sequence of microoperations.).

The advantage of allowing native instructions to execute on a processor is that they can be more efficient and less time consuming than converting a native instruction into a plurality of smaller operations. One of ordinary skill in the art would have been motivated by this advantage to allow for native operations to complete on the processor of Gee. Thus, it would have been obvious to one of ordinary skill in the art at the time of

the invention to implement the execution of native operations on the processor of Gee for the advantage of increased performance.

29. As per claim 2:

Gee and Seal disclosed the processor of claim 1, including a vector table accessible by said decode logic, said vector table including information which specifies whether an instruction is to be replaced by a micro-sequence (Seal: Figure 2 element 24, column 6 lines 60-67 continued to column 7 lines 1-23)(All of the entries in element 24 store pointers to a group of instructions that will replace the instruction. Thus having the same functionality.).

30. As per claim 3:

Gee and Seal disclosed the processor of claim 2 wherein the information is provided to the vector table from a block of memory accessible to the processor by an indirect addressing mode used in a repeat loop comprising at least one instruction (Seal: Figure 10, column 10 lines 34-67 continued to column 11 lines 1-20)(The vector table is initialized with value in a repeat loop shown in figure 10.).

31. As per claim 4:

Gee and Seal disclosed the processor of claim 2 wherein the vector table comprises a plurality of entries and any one entry can be modified independently of the other entries (Seal: Figure 10 element 120, column 10 lines 34-67 continued to column 11 lines 1-20)(Upon initialization, each entry is written independently of each other. Thus having the same functionality.).

32. As per claim 7:

Gee and Seal disclosed the processor of claim 1 wherein the active program counter again switches between the first and second program counters when the micro-sequence is completed (Gee: Figure 2 element 204 and 226, column 8 lines 49-67 continued to column 9 lines 1-52)(Upon the completion of the micro program, another macro java bytecode is fetched to execute. With the micro PC not fetching and executing the micro program, the PC will fetch additional java bytecodes as the active PC.).

33. As per claim 8:

Gee and Seal disclosed the processor of claim 1 wherein the second program counter is used to fetch and decode instructions comprising a micro-sequence and switching between the first and second program counters comprises switching from the first program counter to the second program counter and loading the second program counter with a starting address of the micro-sequence (Gee: Figure 2 elements 204 and 226, column 8 lines 49-67 continued to column 9 lines 1-52)(Figure two shows that the micro PC is used to index into the micro instruction storage to fetch instructions. It's inherent then that the micro PC is given the starting address of the micro sequence of instructions to correctly fetch and execute them.).

34. As per claim 9:

Gee and Seal disclosed the processor of claim 1 wherein a plurality of instructions are replaceable by a corresponding micro-sequence (Gee: Column 8 lines 50-62)(The macro java bytecodes are replaced by a pointer that points to a sequence of micro instructions.).

35. Claims 5-6 are rejected under 35 U.S.C. §103(a) as being unpatentable over Gee et al. (U.S. 6,317,872), in view of Seal (U.S. 6,965,984), further in view of Zaidi (U.S. 6,581,154).

36. As per claim 5:

Gee and Seal disclosed the processor of claim 1.

Gee and Seal failed to teach including a micro-sequence vector table comprising a plurality of entries, each entry corresponding to a separate instruction and associated with a bit indicating whether the corresponding instruction is to be executed by the processor or whether the instruction is to be replaced by a micro-sequence.

However, Zaidi disclosed including a micro-sequence vector table comprising a plurality of entries, each entry corresponding to a separate instruction and associated with a bit indicating whether the corresponding instruction is to be executed by the processor or whether the instruction is to be replaced by a micro-sequence (Zaidi: Figure 2 element 205, column 4 lines 1-7)(Element 205 stores both U ops and S U ops. The S U ops are to be further expanded and the bits associated with them indicate that they are to be replaced by a group of instruction by element 210. The U ops have bits associated with them that indicate no further expansion is needed and that they can be sent directly to the dispatch queue. Thus having the same functionality.).

Gee disclosed a processor that replaces macro java bytecodes with a micro sequence of instructions. Gee disclosed that a java bytecode is essentially a pointer to a sequence of microinstructions (Gee: Column 8 lines 57-59). However, Gee doesn't

disclose the process of the replacement. One of ordinary skill in the art would have been motivated by the lack of the disclosure on the replacement process to find additional details on the process. Zaidi disclosed using a vector table of entries that will replace a macroinstruction with microinstructions. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a vector table to contain pointers to the microinstructions that will replace the java bytecodes.

37. As per claim 6:

Gee, Seal, and Zaidi disclosed the processor of claim 5 wherein at least some of the entries include a reference to a memory location in which a micro-sequence is stored depending if the associated bit indicates that the instruction is to be replaced by a micro-sequence (Zaidi: Figure 2 elements 205 and 210, column 4 lines 1-7)(Element 205 inherently includes information about a memory location that stores the instructions to be replaced.).

38. Claim 15 is rejected under 35 U.S.C. §103(a) as being unpatentable over Gee et al. (U.S. 6,317,872), in view of Seal (U.S. 6,965,984) and in view of Greenberger et al. (U.S. 6,092,179).

39. As per claim 15:

Claim 15 essentially recites the same limitations of claim 1. Claim 15 additionally recites the following limitations:

Gee and Seal additionally disclosed a second processor (Gee: Figure 1 element 100).

Gee and Seal failed to teach a first processor coupled to the second.

However, Greenberger disclosed a first processor coupled to the second (Greenberger: Figure 2 elements 2 and 7, column 3 lines 49-67).

One technique to add new functionality to a processor is to add a co-processor with the added technique (Greenberger: Column 2 lines 1-20). One of ordinary skill in the art would have been motivated to add the combine the processor of Greenberger and Gee for the added functionality of executing macro java bytecodes and replacing them with a micro sequence. Thus, it would have been obvious to one of ordinary skill in the art to combine the two processors for the added functionality of executing java bytecodes.

40. Claims 16-17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Gee et al. (U.S. 6,317,872), in view of Seal (U.S. 6,965,984), in view of Greenberger et al. (U.S. 6,092,179), further in view of Zaidi (U.S. 6,581,154).

41. As per claim 16:

Gee, Seal, and Greenberger disclosed the system of claim 15.

Gee, Seal, and Greenberger failed to teach wherein said second processor further includes a micro-sequence vector table comprising a plurality of entries, each entry corresponding to a separate instruction and including a field that indicates whether the corresponding instruction is to be executed by the second processor or whether the instruction is to be replaced by a micro-sequence.

However, Zaidi disclosed wherein said second processor further includes a

micro-sequence vector table comprising a plurality of entries, each entry corresponding to a separate instruction and including a field that indicates whether the corresponding instruction is to be executed by the second processor or whether the instruction is to be replaced by a micro-sequence (Zaidi: Figure 2 element 205, column 4 lines 1-7)(Element 205 stores both U ops and S U ops. The S U ops are to be further expanded and the bits associated with them indicate that they are to be replaced by a group of instruction by element 210. The U ops have bits associated with them that indicate no further expansion is needed and that they can be sent directly to the dispatch queue. Thus having the same functionality.).

Gee disclosed a processor that replaces macro java bytecodes with a micro sequence of instructions. Gee disclosed that a java bytecode is essentially a pointer to a sequence of microinstructions (Gee: Column 8 lines 57-59). However, Gee doesn't disclose the process of the replacement. One of ordinary skill in the art would have been motivated by the lack of the disclosure on the replacement process to find additional details on the process. Zaidi disclosed using a vector table of entries that will replace a macroinstruction with microinstructions. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a vector table to contain pointers to the microinstructions that will replace the java bytecodes.

42. As per claim 17:

Claim 17 essentially recites the same limitations of claim 6. Therefore, claim 17 is rejected for the same reasons as claim 6.

Response to Arguments

43. The arguments presented by Applicant in the response, received on 7/17/2006 are not considered persuasive.

44. Applicant argues that "Gee fails to teach Wherein an instruction is replaced by a micro-sequence comprising one or more instructions and the active program counter switches between the first and second program counters based on a micro-sequence-active bit" for claims 1 and 15

This argument is found to be persuasive. However, a new grounds of rejection has been given due to the amendment.

45. Applicant argues that "Gee fails to teach determining whether said instruction is to be executed or replace by a group of other instructions" for claim 10.

This argument is not found to be persuasive for the following reason. It's inherent that there is a determining step since each bytecode will be chosen to be replaced by a group of other instructions.

46. Applicant argues that "Zaidi fails to teach determining whether said instruction is to be executed or replace by a group of other instructions" for claims 10 and 22.

This argument is not found to be persuasive for the following reason. Zaidi clearly shows a determining step in element 203 that shows an instruction being replaced by a group of other instructions.

47. Applicant argues that "Seal failed to teach a vector table comprising a plurality of entries, each entry corresponding to a separate instruction and including a first field indicating whether the corresponding instruction is to be executed by the electronic

device or whether the instruction is to be replaced by a predetermined group of instructions stored in memory" for claim 18.

This argument is not found to be persuasive for the following reason. The vector table cited is element 24 in figure 2. The table inherently contains a field that is inclusive within the pointers that tells that the bytecode instruction will be replaced by a predetermined group of instructions stored in element 26.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner
Art Unit 2183

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100